Initiallization timing parameters

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Parameter | Value | | Unit | Comment |
| **Min** | **Max** |
| tINIT0 | - | 20 | ms | Maximum voltage-ramp time |
| tINIT1 | 200 | - | us | Minimum RESET\_n LOW time after completion of voltage ramp |
| tINIT2 | 10 | - | ns | Minimum CKE low time before RESET\_n high |
| tINIT3 | 2 | - | ms | Minimum CKE low time after RESET\_n high |
| tINIT4 | 5 | - | tCK | Minimum stable clock before first CKE high |
| tINIT5 | 2 | - | us | Minimum idle time before first MRW/MRR command |
| tZQCAL | 1 | - | us | ZQ calibration time |
| tZQLAT | Max(30ns, 8tCK) | - | ns | ZQCAL latch quiet time. |
| tCKb | Note \*1,2 | Note \*1,2 | ns | Clock cycle time during boot |

NOTE 1 Min tCKb guaranteed by DRAM test is 18 ns.  
NOTE 2 The system may boot at a higher frequency than dictated by min tCKb. The higher boot  
frequency is system dependent.

Boot frequency guaranteed by DRAM test is 1/18 \*1.0e9 约 55.5Mhz。

gate training : 调整read 过程dqsck。

Read commond发出后，经过(RL\*tCK)+tDQSCK时间后，收到lpddr4返回的第一个有效DQS上升沿，这样提前两个DDR clock cycle即可保证可以接收完整read back的信息。

**tDQSCK\_rank2rank Timing Table**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Parameter** | **Symbol** | **Min/Max** |  | | | | | | **Unit** | **Note** |
| **Read Timing** | | | **1600** | **1866** | **2133** | **2400** | **3200** | **4267** |
| CK to DQS Rank to Rank variation | tDQSCK\_rank2rank | Max | 1 | | | | | | ns | 1,2 |

NOTE 1 The same voltage and temperature are applied to tDQS2CK\_rank2rank.  
NOTE 2 tDQSCK\_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies

怀疑DDR clock stop后，再enable clock，两次不一定同phase，所以Tdqsck可能发生变化。需请教Memory 厂商。JEDEC stander没有说明。